HP 3000 SERIES III
COMPUTER SYSTEM
MANUAL OF STAND-ALONE DIAGNOSTICS

STAND-ALONE
SYSTEM CLOCK DIAGNOSTIC

Diagnostic No. D426A

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I. INTRODUCTION

The Stand-Alone System Clock Diagnostic verifies the functional level operation of the System Clock/FLI PCA, part no. 30135-60063. The diagnostic is capable of diagnosing the problems related to bit misconfiguration of the Count Register (CR), Limit Register (LR), and Count Rate Selector Register. Additionally, the interrupts and overflow conditions are tested as well as Control I/O (CIO) command bits and status bits associated with the System Clock/Fault Logging interface.

II. MINI-OPERATING INSTRUCTIONS

A. Operations

1. Cold Load Diag File# (Associated with System Clock Diagnostic D426A) from non-CPU Cold Load Tape.
2. Respond to Speed-Sense by asserting "CR" at the console.
3. Respond to dialogue at the console.

B. Switch Register Options

Bit#	Function
0	Select External Switch Register
1	Set To Change Section Switch Register
2	Spare
3	Spare
4	Spare
5	Loop Current Section
6	Spare
7	Output To Line Printer (if configured in SDUPII)
8	Spare
9	Suppress Non-Error Messages
10	Suppress Error Messages
11	Loop On Last Executed Step
12	Halt On Error
13	Halt At The End Of Step
14	Halt At The End Of Section
15	Halt After A Complete Program Cycle

C. Section Switch Register Options

Bit#	Function
0	Reconfigure
1	Select Section 1
2	Select Section 2
3	Select Section 3
4	Select Section 4
5-15	Spare

D. Halt Assignments

No.(octal)	Function
0	Halt For Switch Entry (External Register)
1	Halt For Switch Entry (Section Select)
2	Halt For Switch Entry (Restore Ext. Reg.)
3	Halt On Error Count Reached
4-11	Spare
12	Halt For Error
13	Halt After Step
14	Halt After Section
15	Halt After Complete Program Cycle
16-17	Spare

III. REQUIREMENTS

A. Hardware

The hardware required to run the System Clock Diagnostic is the minimum HP 3000 Series III computer system.

B. Software

The Stand-Alone Diagnostic Utility Program (SDUPII) is required to create the Stand-Alone Diagnostic tape. The tape is comprised of the Cold Load program, the Relocating Loader, and one or more diagnostic programs including the Stand-Alone System Clock Diagnostic. All the programs are coded in System Programming Language (SPL).

IV. DETAILED OPERATING INSTRUCTIONS

A. Operating Instructions

The following are the instructions for loading, executing, and configuring the Stand-Alone System Clock Diagnostic:

1. Cold Load by entering %3006 into the Switch Register and simultaneously depressing the "LOAD" and "ENABLE" switches on the CPU front panel.

2. Select an appropriate Diagnostic File # (associated with the System Clock Diagnostic) and enter the number into the Switch Register. Depress the "RUN" switch. The diagnostic tape supplied is identified by file names and their respective file position on the tape. The selected program is now loaded into memory. The tape rewinds at the end of program load.

3. The diagnostic program is now executable.

4. Depress the console "RETURN" key to respond to the Speed-Sense. Then, the program prints the diagnostic header information and requests the necessary parameters to begin the diagnostic cycle.

B. Options

Under the System Clock Diagnostic, the operator can control the test sections to be executed; control halts on an error after sections or steps or upon program completion; control suppression of error and nonerror messages; and control loop on a specific test step. These control options may be entered when the program requests for a specific option entry via the test dialogue.

It should be noted however, that the program has been preconfigured to be executable in its best load and go configuration when the options are defaulted (execute all four sections).

1. The following describes the options associated with each bit of the Switch Register. The program asks the operator to set the Switch Register on the front panel. It's value equals zero when in default.

Q02 SELECT SWITCH REGISTER OPTIONS

Bit#	Function
0	Select External Switch Register
1	Set to change Section Switch Register
2	Spare
3	Spare
4	Spare
5	Loop Current Section
6	Spare
7	Output to Line Printer (if configured in SDUPII)
8	Spare
9	Suppress Non-Error Messages
10	Suppress Error Messages
11	Loop on last executed step
12	Halt on error
13	Halt at the end of step
14	Halt at the end of section
15	Halt after a complete program cycle

If bits 0 and 1 are either 00 or 01, then the previously configured values are used for the execution. In the case for an initial state, the pre-defined values (best load and go conditions) for both

"Switch Register Options" and "Section Switch Register Options" are used.

If bits 0 and 1 are 10, then only the Switch Register content will be altered and the previously configured Section Switch Register Options are used for the execution. It's value equals %074000 when in default.

If bits 0 and 1 are 11, then the contents of both the "Switch Register" and "Section Switch Register" are altered after an appropriate option entry.

2. The following describes the options associated with each bit of the Section Switch Register. The program asks the operator to set a number on the Section Switch Register.

Q03 SELECT SECTION SWITCH REGISTER OPTIONS

Bit#	Function
0	Reconfigure
1	Select Section 1
2	Select Section 2
3	Select Section 3
4	Select Section 4
5-15	Spare

When "RUN" is depressed, control passes back to Q002 Select Switch Register Options when both bits 0 and 1 are set. Otherwise, the program continues.

3. The following message asks the operator to enter the DRT number.

Q001 ENTER SYSTEM TIMER DEVICE#

The operator types the DRT number on the console in octal form and "RETURN".

4. The following message asks the operator to enter the maximum number of errors to be counted.

Q004 ENTER MAXIMUM ERROR COUNT

The operator types the DRT number on the console in octal form and "RETURN".

C. Halts and Message Tables

1. Halt Assignments

When a program halts, a code is displayed in the Current Instruction Register (CIR). This is displayed as 0 011 000 011 11X XXX, where "X XXX" is the halt number.

Bits 12-15 (CIR-Octal)	Assignments
0	Halt for Switch Register entry (Ext.)
1	Halt for Switch Register entry (Section Select)
2	Halt for Switch Register entry (Restore Ext.)
3	Halt on error count reached
4-11	Spare
12	Halt for error
13	Halt after step
14	Halt after section
15	Halt after a complete program cycle
16-17	Spare

2. There are four types of message classifications; D, E, P, and Q classes.

D-Class

Messages that describe program boundaries. Some operator intervention is required.

E-Class

Messages that are related to error numbers. Some operator intervention is required.

P-Class

Messages that describe the test completion of a section or step. Some operator intervention is required.

Q-Class

Messages that request some parameter entry be made. Operator intervention is required.

2.1 Actual Message Descriptor

2.1.1 D01 SYSTEM CLOCK DIAGNOSTIC (D426X.YY.ZZ)

Header information for this program where:
X = Version Letter
YY = Update Number
ZZ = Fix Number

2.1.2 D02 HALT: PROGRAM CYCLE: PASS = XXXXX

This message indicates the number of test passes the program has completed for those sections selected.

2.1.3 D03 HALT: COMPLETE PROGRAM CYCLE

This message is output whenever bit number 15 of the Switch Register Option is set (1).

2.1.4 Q01 ENTER SYSTEM TIMER DEVICE #=

Program request for Timer DRT entry.

2.1.5 Q02 SELECT SWITCH REGISTER OPTIONS

Program is requesting option entry as described in Section IV.B.1.

2.1.6 Q03 SELECT SECTION SWITCH REGISTER OPTIONS

Program is requesting option entry as described in Section IV.B.2.

2.1.7 Q04 ENTER MAXIMUM ERROR COUNT #=

Program is requesting the maximum error count to be entered. The maximum count which can be entered is 9999.

2.1.8 Q05 RESTORE SWITCH REGISTER OPTIONS
(Same option entry as in Q02 above.)

2.1.9 P01 SECTION XX

This message indicates the test section number which will be executed.

2.1.10 P03 END SECTION XX

This message indicates the test section number which has just been completed.

2.1.11 P04 END STEP XXX

This message indicates that the test step in execution has just been completed.

2.1.12 P05 HALT: STEP XXX

This message indicates that the computer is an a halt state after completing the indicated step.

2.1.13 P06 HALT: SECTION XX

This message indicates that the program has halted after completing the indicated section.

2.1.14 P08 ERROR: HALT STEP XXX

This message indicates an error occurrence within the test step indicated.

2.1.15 P09 MAX. ERROR COUNT REACHED

This message indicates that the entered or predefined error count has been reached. The computer will be in a halt state.

2.1.16 Exxx

This message indicates the appropriate error number associated with the actual error.

2.1.17 STATUS IS = X XXX XXX XXX XXX XXX

This message displays the actual data associated to the test.

2.1.18 SHOULD BE = X XXX XDD DDD XXD XXX

This message displays the expected values. "D" indicates "don't care" bits.

D. Pre-Configuration Options

1. The diagnostic program has been pre-configured to execute in best load and go configuration using the options described in Sections IV.B.1 and IV.B.2. The pre-configured values can be altered when the diagnostic cold load tape is being created under SDUPII.

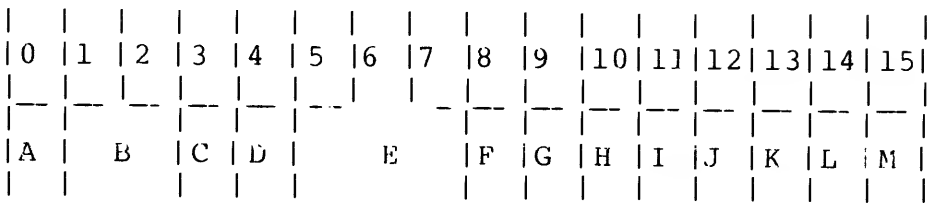
   The External Switch Register and Select Section Switch Register are initialized to 1 and %74000 respectively when defaulted.

2. The following are the DB Locations containing data that can be changed during pre-configuration using SDUPII.

DB+0	Switch Register Setting
DB+1	Section Register Setting
DB+2	Version and Update level
DB+3	System Clock DRT Number
DB+4	Maximum Error Print Count

E. Control and Status Word Formats

1. Control Word Format



A Master Clear. To function as Master Clear, bit 3 of this word must be reset.

B CR Count Rate. Three bits (0, 1, and 2) determine the count rate for the CR when bit 3 is set (1). Determine count rate selection from Table 1.1.

C Master Clear/Count Rate Selection. When set (1), this bit designates that bits 0-2 will be used as the selection of the Count Rate for the CR. When reset (0), this bit enables bit 0 to function as Master Clear and bits 1 and 2 are not used.

D Unused.

E Selective Interrupt Clear. These three bits (5, 6, and 7) selectively clear each process which generates an interrupt request. Table 1.2 lists the necessary bit patterns to selectively clear each interrupt process.

F Reset CR After LR=CR Interrupt. When this bit is set (1), the CR to be reset after an interrupt request is generated by the LR=CR process.

G LR/CR Function Selection. When this bit is reset (0), WIO commands address the Limit Register (LR). When this bit is set (1), RIO and WIO address the Count Register (CR). The RIO command always addresses the CR.

H Clear All Interrupts. When this bit is set (1), all logic on the subsystem PCA which generates an interrupt request to the CPU will be cleared.

I Unused.

J Unused.

K Unused.

L Unused.

M Enable Clock Interrupts. When this bit is reset (0), all interrupt requests from the system clock logic to the CPU are inhibited. When this bit is set (1), all interrupt requests from the system clock logic to the CPU are enabled.

Table 1.1 Count Rate Selection

Control Word Bits			Count Rate
0	1	2	
0	0	0	Unused
0	0	1	10 microseconds
0	1	0	100 microseconds
0	1	1	1 millisecond
1	0	0	10 milliseconds
1	0	1	100 milliseconds
1	1	0	1 second
1	1	1	10 seconds

Table 1.2 Interrupt Clear Selection

Control Word Bits			Interrupt Process Cleared
5	6	7	
0	0	0	None
0	0	1	LR = CR
0	1	0	LR = CR Overflow
0	1	1	I/O System Interrupt (SIN)
1	0	0	Unused
1	0	1	Unused
1	1	0	Unused
1	1	1	Unused

2. Status Word Format

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	B	C			D	E	F	G	H	I	J	K	L	M	N

A SIO OK. This bit is permanently reset (0), indicating that the subsystem is incapable of operating in SIO mode.

B RIO, WIO OK. This bit is permanently set (1), indicating that the subsystem is capable of executing RIO and WIO commands.

C CR Count Rate. These three bits reflect the count rate of the CR. The count rate is determined by Control Word bits 0-2 as shown in Table 1.2.

D Unused

E Unused

F Unused

G Unused

H Unused

I LR=CR. When this bit is set (1), it indicates that the count in the LR has been reached by the CR and an interrupt request is generated.

J LR=CR Overflow. When this bit is set (1), it indicates that the CR has reached the count in the LR two times without being serviced by an interrupt and an interrupt request is generated.

K Unused

L I/O System Interrupt. When this bit is set (1), it indicates that the subsystem PCA has received a Set Interrupt command (SIN) from the CPU and an interrupt request is generated.

M LR/CR Selection Status. When this bit is reset (0),it indicates that WIO commands address the LR. When this bit is set (1), it indicates that WIO commands address the CR.

N Control Word Bit Selection Status. When this bit is set (1), it indicates that the CR is reset after an interrupt request is generated by the LR=CR signal.

V. DETAILED TEST DESCRIPTION

The Stand-Alone System Clock Diagnostic is divided into four test sections and each test section is divided into several test steps. All test steps are described below.

1. Section 1

1.1 STEP 101

Tests setting the CR and LR using all possible 8-bit patterns. The CRS is set to a time base of 1.0 millisecond. Initially, CR=0 and LR=CR+1. Then, both LR and CR are incremented progressively with a TIO in a loop until CR=%377.

1.1.1 Step 101 Error Codes and Messages

NO INTERRUPT AFTER INT. REQUEST AND TIME-OUT
E101
  LR COUNTER = 0 000 000 0XX XXX XXX
The error message contains the LR counter value when the counter time expired.

E707
  STEP NUM. = 0 000 000 001 000 001
  DEV. NUM. = 0 000 000 0XX XXX XXX
Displayed Device Number is for the non-responding device.

E102
  CR COUNTER = 0 000 000 0XX XXX XXX
  LR COUNTER = 0 000 000 0YY YYY YYY
The error message output when the compare (LR and CR) error occured.

1.2 STEP 103

Tests CR=LR interrupt with 1.0 millisecond time base. Initially, LR=1 and CR=0.

1.2.1 Step 103 Error Codes and Messages

E103
  NO INTERRUPT AFTER LR=CR
The error message indicates that an interrupt for LR=CR was not generated within the alloted time.

E104
  DEV.STAT. = X XXX XXX XXX XXX XXX
  SHOULD BE = 0 101 100 100 100 001
This error message is generated when the LR=CR interrupt is not noted in Device Status.

E106
  STATUS IS = X XXX XXX XXX XXX XXX
  SHOULD BE = 0 000 000 000 000 000

1.3 STEP 105

Tests for overflow when CR>LR with 100 microseconds time base. The program waits approximately 700 microseconds to get the overflow status.

1.3.1 Step 105 Error Codes and Messages

E105
  STATUS IS = X XXX XXX XXX XXX XXX
  SHOULD BE = 0 101 000 100 110 001

2. Section 2

This section tests all Count Rates for CR=LR.

Table 2.1 Execute Table For Steps 202 Thru 210

Step No.	Increment	CRS (Binary)	CR (Octal)	LR (Octal)	Time Interval
202	10 usec	001	000000	000012	100 usec
203	100 usec	010	000000	000004	400 usec
204	1.0 msec	011	000000	000004	4.0 msec
205	10 msec	100	000000	000004	40 msec
206	100 msec	101	000000	000004	400 msec
207	1.0 sec	110	000000	000004	4.0 sec
210	10 sec	111	000000	000004	40 sec

2.2 Steps 201-210 Error Codes and Messages

Table 2.1 lists all possible error messages for Section 2 when LR is not equal to CR during execution.

2.3 STEP 201 - Unused.

2.4 STEP 202

E202
STATUS IS = X XXX XXX XXX XXX XXX
SHOULD BE = 0 100 100 100 100 000

2.5 STEP 203

E203
STATUS IS = X XXX XXX XXX XXX XXX
SHOULD BE = 0 101 000 100 100 000

2.6 STEP 204

E204
STATUS IS = X XXX XXX XXX XXX XXX
SHOULD BE = 0 101 100 100 100 000

2.7 STEP 205

E205
STATUS IS = X XXX XXX XXX XXX XXX
SHOULD BE = 0 110 000 100 100 000

2.8 STEP 206

E206

STATUS IS = X XXX XXX XXX XXX XXX

SHOULD BE = 0 110 100 100 100 000

2.9 STEP 207

E207

STATUS IS = X XXX XXX XXX XXX XXX

SHOULD BE = 0 111 000 100 100 000

2.10 STEP 210

E210

STATUS IS = X XXX XXX XXX XXX XXX

SHOULD BE = 0 111 100 100 100 000

3. Section 3

This section tests CIO command bits associated with the System Clock.

3.1 STEP 302

This test validates CIO command bits 5-7 (001) which reset LR=CR interrupt.

3.1.1 Step 302 Error Message

E302

STATUS IS = X XXX XXX XXX XXX XXX

SHOULD BE = 0 101 000 100 000 000

This message is given when bit 10 of the status word becomes set (1) after a LR=CR condition.

3.2 STEP 304

This test validates CIO command bits 5-7 (010) which test CR>LR overflow.

3.2.1 Step 304 Error Messages

E304

STATUS IS = X XXX XXX XXX XXX XXX

SHOULD BE = 0 101 000 100 000 000

This message is given when bit 11 of the status word is set (1) after a CR>LR condition.

3.3 STEP 306

This test validates CIO command bits 5-7 (011) which reset the interrupt generated by a Set Interrupt instruction (SIN).

3.3.1 Step 306 Error Messages

E306
STATUS IS = X XXX XXX XXX XXX XXX
SHOULD BE = 0 101 000 100 110 100
This message is given when the SIN instruction is executed and bit 13 of the status word is not set (0).

E307
STATUS IS = X XXX XXX XXX XXX XXX
SHOULD BE = 0 101 000 100 110 000
This message is given when the reset SIN interrupt command is issued and bit 13 of the status word is set (1).

3.4 STEP 310

This test verifies that the Master Reset command clears all interrupts.

3.4.1 Step 310 Error Message

E310
STATUS IS = X XXX XXX XXX XXX XXX
SHOULD BE = 0 101 100 100 000 000
This message is given when LR=CR and CR>LR overflow interrupts are forced and the Master Reset command is issued to reset these interrupts. Status word bits 10 and 11 should reflect the change from set (1) to reset (0).

3.5 STEP 312

This test validates the Master Reset for the entire board. A testcondition is not set up. Just a one-shot MR command is issued.

3.5.1 Step 312 Error Message

E312
STATUS IS = X XXX XXX XXX XXX XXX
SHOULD BE = 0 101 100 100 000 000
This message is given when read status is not equal to expected.

3.6 STEP 314

This test reset CR after each interrupt by using CIO command bit 8.

3.6.1 Step 314 Error Message

```
E314
  STATUS IS = X XXX XXX XXX XXX XXX
  SHOULD BE = 0 000 000 000 000 000
```

This message is given when the content of the CR is not equal to zero after the reset LR=CR interrupt command is issued.

3.7 STEP 316

This test validates Clock Interrupt Mask bit 15.

3.7.1 Step 316 Error Message

```
E316
  NO INTERRUPT AFTER LR=CR
```

The error code indicates that the LR=CR interrupt did not occur within the time alloted after enabling the clock interrupt (CIO bit 15).

4. Section 4

This section tests various status bits associated with the CIO commands for the System Clock.

4.1 STEP 402

This step validates status word bit 0 always being reset (0). (SIO not allowed.)

4.1.1 Step 402 Error Messages

```
E402
  STATUS IS = X XXX XXX XXX XXX XXX
  SHOULD BE = 0 101 100 100 100 000
```

This message is given when, at any time during 1000 (decimal) loops, a status error occurs. (Bit 0 set.)

4.2 STEP 404

This test validates status word bit 1 always being set (1). RIO and WIO are allowed.

4.2.1 Step 404 Error Message

```
E404
  STATUS IS = X XXX XXX XXX XXX XXX
  SHOULD BE = 0 101 100 100 100 000
```

This message is given when, at any time during 1000 (decimal) loops, a status error occurs. (Bit 1 not set.)

4.3 STEP 406
This test validates setting status word bits 2-4 to 000 by issuing CIO command bits 0-2 with 000.

4.3.1 Step 406 Error Message

E406
STATUS IS = X XXX XXX XXX XXX XXX
SHOULD BE = 0 100 000 100 000 001

4.4 STEP 407
This test validates setting status word bits 2-4 to 001 by issuing CIO command bits 0-2 with 001.

4.4.1 Step 407 Error Message

E407
STATUS IS = X XXX XXX XXX XXX XXX
SHOULD BE = 0 100 100 100 000 001

4.5 STEP 410 - Unused

4.6 STEP 411
This test validates setting status word bits 2-4 to 011 by issuing CIO command bits 0-2 with 011.

4.6.1 Step 411 Error Message

E411
STATUS IS = X XXX XXX XXX XXX XXX
SHOULD BE = 0 101 100 100 000 001

4.7 STEP 412
This test validates setting status word bits 2-4 to 100 by issuing CIO command bits 0-2 with 100.

4.7.1 Step 412 Error Message

E412
STATUS IS = X XXX XXX XXX XXX XXX
SHOULD BE = 0 110 000 100 000 001

4.8 STEP 413
This test validates setting status word bits 2-4 to 101 by issuing CIO command bits 0-2 with 101.

4.8.1 Step 413 Error Message

```
E413
  STATUS IS = X XXX XXX XXX XXX XXX
  SHOULD BE = 0 110 100 100 000 001
```

4.9 STEP 414

This test validates setting status word bits 2-4 to 110 by issuing CIO command bits 0-2 with 110.

4.9.1 Step 414 Error Message

```
E414
  STATUS IS = X XXX XXX XXX XXX XXX
  SHOULD BE = 0 111 000 100 000 001
```

4.10 STEP 415

This test validates setting status word bits 2-4 to 111 by issuing CIO command bits 0-2 with 111.

4.10.1 Step 415 Error Message

```
E415
  STATUS IS = X XXX XXX XXX XXX XXX
  SHOULD BE = 0 111 100 100 000 001
```

4.11 STEP 422

This test validates status word bit 15 by causing a LR=CR condition and then issuing a CIO command to reset CR after LR>CR interrupt which sets bit 15 (1).

4.11.1 Step 422 Error Message

```
E422
  STATUS IS = X XXX XXX XXX XXX XXX
  SHOULD BE = 0 101 000 100 000 011
```

This message is given when the CIO command to reset CR after LR=CR interrupt is issued but bit 15 of the status word is not set (0).

4.12 STEP 424

This test validates that status word bit 14 is equal to 0 when bits 9 and 12 (command word) are equal to 0 and 1 respectively.

4.12.1 Step 424 Error Message

E424
STATUS IS = X XXX XXX XXX XXX XXX
SHOULD BE = 0 101 100 100 000 000
This message is given when an LR=CR condition is forced and then a CIO command to access LR is issued.

4.13 STEP 426

This test validates that status word bit 14 is set (1) when bits 9 and 12 (command word) are are both set (1).

4.13.1 Step 426 Error Message

E426
STATUS IS = X XXX XXX XXX XXX XXX
SHOULD BE = 0 101 100 100 000 010
This message is given when an LR=CR condition is forced and then a CIO command to access LR is issued, but after after issuing a TIO command to sense that device status bit 14 is not set (0).